

TS02EE

Specifications

Nomura Engineering Co., Ltd.

Please do not apply this product in a way that its failures and errors may involve human lives..
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Introduction

TS02EE transceiver module consists of microcontroller, receiver and transmitter sections, all in one package. Equipped with a flexible antenna and 20-pin interface connector, it can be easily integrated into a compact case.

This module is applied for various wireless systems like remote control, telemetry, data transfer, security and so forth.

Features

RoHS compliant

Compact size

Excellent electronic characteristics

Low voltage operation down to 2.1V DC

Electrical Characteristic

General

Oscillation system	PLL frequency synthesizer according to referece crystal clock
Communication	Two way
Transmitter frequency	434.0500 ~ 434.5375 MHz
Number of channels	40
Channel step	12.5 kHz
Duty cycle class	100% (Class 4)
Frequency stability	± 3.5 ppm (-20 to + 70 degree C)
Data rate	2500 bps
Supply voltage	2.1 - 7.0 V DC
Consumption current	Typ. 14 mA at 2.1 - 7.0 V DC during receiving Typ. 24 mA at 2.1 - 7.0 V DC during transmitting
Dimension	53 x 30 x 6.5 mm (excluding protrusion)
Weight	15g
Operating temperature range	-20 to + 70 degree C
Storage temperature range	-30 to + 80 degree C

Transmitter

RF output power	10 mW
Start up time	TBD ms (from power on)
Deviation	< ±2.1 kHz (PN9 4800 bps)
Spurious emission	< -54 dBm (47-74 M, 87.5-118 M, 470-862 M)* < -36 dBm (others below 1 GHz)* < -30 dBm (> 1 GHz)*
Adjacent channel power	< -37 dBm

Receiver

Receiver class	2
Receiver system	Double superheterodyne
Sensitivity	Typ. -118 dBm (12 dB SINAD AF at CCITT 1 kHz filter on) TBD dBm (BER 1% at 4800bps)
Spurious response rejection	≥ -44 dBm*
Adjacent channel selectivity	60 dB (±12.5 kHz)
Blocking	84 dB
Spurious radiation	< -60 dBm @ < 1GHz {< -57 dBm} < -50 dBm @ > 1GHz {<-47dBm}

* same as ETSI spec. limit

* { } : standard

compliance with below;

EMC EN301 489-1, -3

R&TTE EN300 220-1

Frequency Table

送受信周波数とチャンネル番号の関係を右テーブルに示した。

CH	Freq.(MHz)
1	434.0500
2	434.0625
3	434.0750
4	434.0875
5	434.1000
6	434.1125
7	434.1250
8	434.1375
9	434.1500
10	434.1625
11	434.1750
12	434.1875
13	434.2000
14	434.2125
15	434.2250
16	434.2375
17	434.2500
18	434.2625
19	434.2750
20	434.2875
21	434.3000
22	434.3125
23	434.3250
24	434.3375
25	434.3500
26	434.3625
27	434.3750
28	434.3875
29	434.4000
30	434.4125
31	434.4250
32	434.4375
33	434.4500
34	434.4625
35	434.4750
36	434.4875
37	434.5000
38	434.5125
39	434.5250
40	434.5375

Software specifications

Maintenance

Measurement Procedures

Theory of Operations

TS02E module consists of baseband processor section, receiver section, PLL frequency synthesizer section, modulation section, transmitter section, antenna switch section, power supply section.

The baseband processor section is mainly a microcontroller, handling receiving and transmitting baseband signals and peripheral interfaces. A received signal is sliced into logic signal and fed into the microcontroller. The received data is decoded according to designated protocol and only effective data is taken out by error check code. Adding frame data of preamble, error check code, etc., transmit data is encoded according to designated protocol and the carrier is modulated.

TS02E moduleはベースバンド処理部、受信部、PLL周波数シンセサイザ部、変調部、送信部、アンテナスイッチ部および電源部より構成される。

ベースバンド処理部はローパワーマイクロコントローラにより、受信データのデコードおよび送信データのエンコードが行われる。

受信データは決められたプロトコルに従ってデコード処理が行われ、誤りチェック符号などにより有効なデータのみが取り出される。また、送信データは誤りチェック符号などが付加され当社の決められたプロトコルに従ってエンコード処理が行われ、キャリアの変調が行われる。

The receiver section consists of SAW band pass filter Z1, 1st mixer Q1 and Q2, 1st 21.70 MHz crystal filter, IF IC U2, 2nd 450 kHz ceramic filter Z2, ceramic discriminator X2 and so forth. The signal received from an antenna is input to the SAW band pass filter to remove 1st IF image frequency and limit bandwidth. The received signal, passing the antenna switch, is fed into the 1st mixer. At the 1st mixer, the signal is mixed with a lower injection local signal, which is lower than the received signal for 21.7 MHz, and the frequency is converted to 21.70 MHz 1st IF signal at conversion gain of about 17 dB. The 1st IF 21.70 MHz signal is fed into the 21.70 MHz crystal filter, where the 2nd IF image frequency is removed and the band is limited. The signal is input to IF IC U2, mixed with 21.250 MHz 2nd local signal, converted to 450 kHz 2nd IF signal. The 450 kHz 2nd IF signal is fully amplified, then after passing remitter, the ceramic discriminator changes it to baseband signal and the data slicer changes it to logic signal. The IF IC U2 outputs RSSI (Received Signal Strength Indicator) signal and it is input to microcontroller U4.

受信部はSAW filter、LAN、第一ミキサ、

アンテナより得られた受信信号はSAW filterにより1st IF image frequencyの除去と帯域制限が行われ、antenna switchを通して1st mixerに供給される。1st mixerでは受信信号より-21.7MHz低いlower injection local signalとミキシングされ、およそ17dBのconversion gainで21.70 MHzの1st IF signalへ周波数変換が行われる。1st IFの21.70 MHzは1st 21.70 MHz crystal filterに供給され、

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2nd IF image frequencyの除去と帯域制限が行われる。更に、IF IC U2に供給され、21.250MHzの2nd local signal とミキシングされ、450kHzの2nd IF signal に変換されます。450kHzの2nd IF signal は十分に増幅され、リミッターを通過後ceramic discriminator によりベースバンド信号に変換されdata slicer によりlogic signal に変換されます。また、IF IC U2はreceiver signal strength indicator (RSSI) signal を出力、microcontroller U4に供給されます。

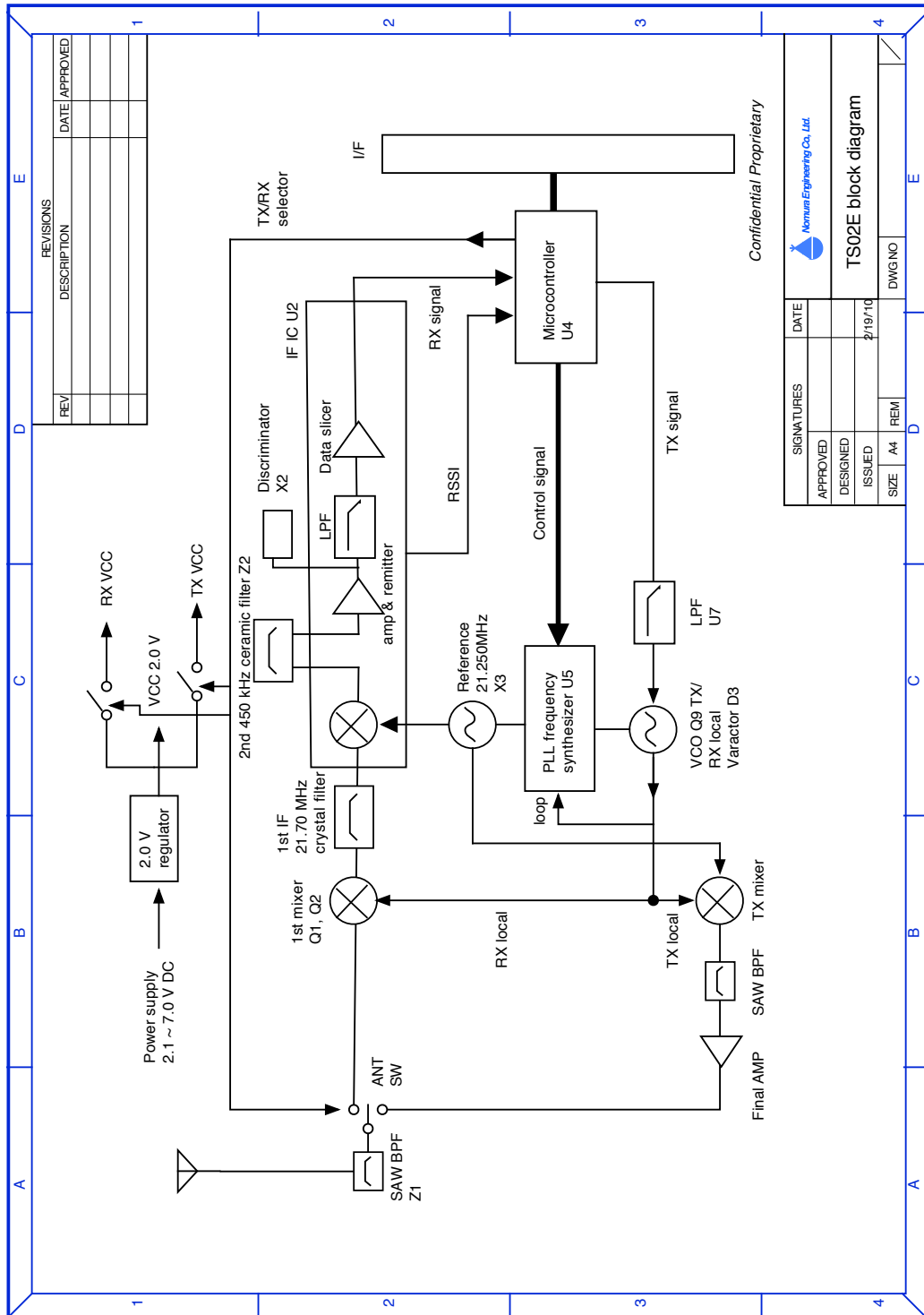
The PLL frequency synthesizer section consists of PLL IC U5, 21.250 MHz reference clock oscillator X3, VCO Q9, lowpass filter U7. The transmit data output by microcontroller U4 is band-limited at lowpass filter and modulated at the VCO to meet the standard of occupied bandwidth and adjacent channel leakage power. The varactor forms PLL frequency synthesizer loop and controls VCO oscillation to get a required frequency. The signals generated by VCO are received local signal and transmit local signal, and the frequencies are -21.70 MHz and -21.25 MHz, respectively.

The transmit local signal is mixed with 21.250 MHz offset frequency to get transmit frequency. The signal is fed into SAW band pass filter to remove spurious emission. Then it is fed into the final AMP to get the output of about -11 dB. Passing the antenna switch, it is fed into the SAW band pass filter to remove spurious emission again.

microcontroller U4より出力される送信データは occupied bandwidth and adjacent channel leakage power の規格を満足する為に、lowpass filter U7で帯域制限が行われ、varactor D3にて変調が行われる。また、varactor D3はPLL frequency synthesizer loop を形成し、VCOの発振周波数を制御して所望の周波数を得ている。VCOにて生成する信号は、受信ローカル信号として受信周波数の-21.70MHzを、送信周波数として送信周波数-21.25MHzの送信ローカル信号を得ている。送信ローカル信号は21.250MHzのオフセット周波数とミキシングアップを行い、送信周波数を得ている。

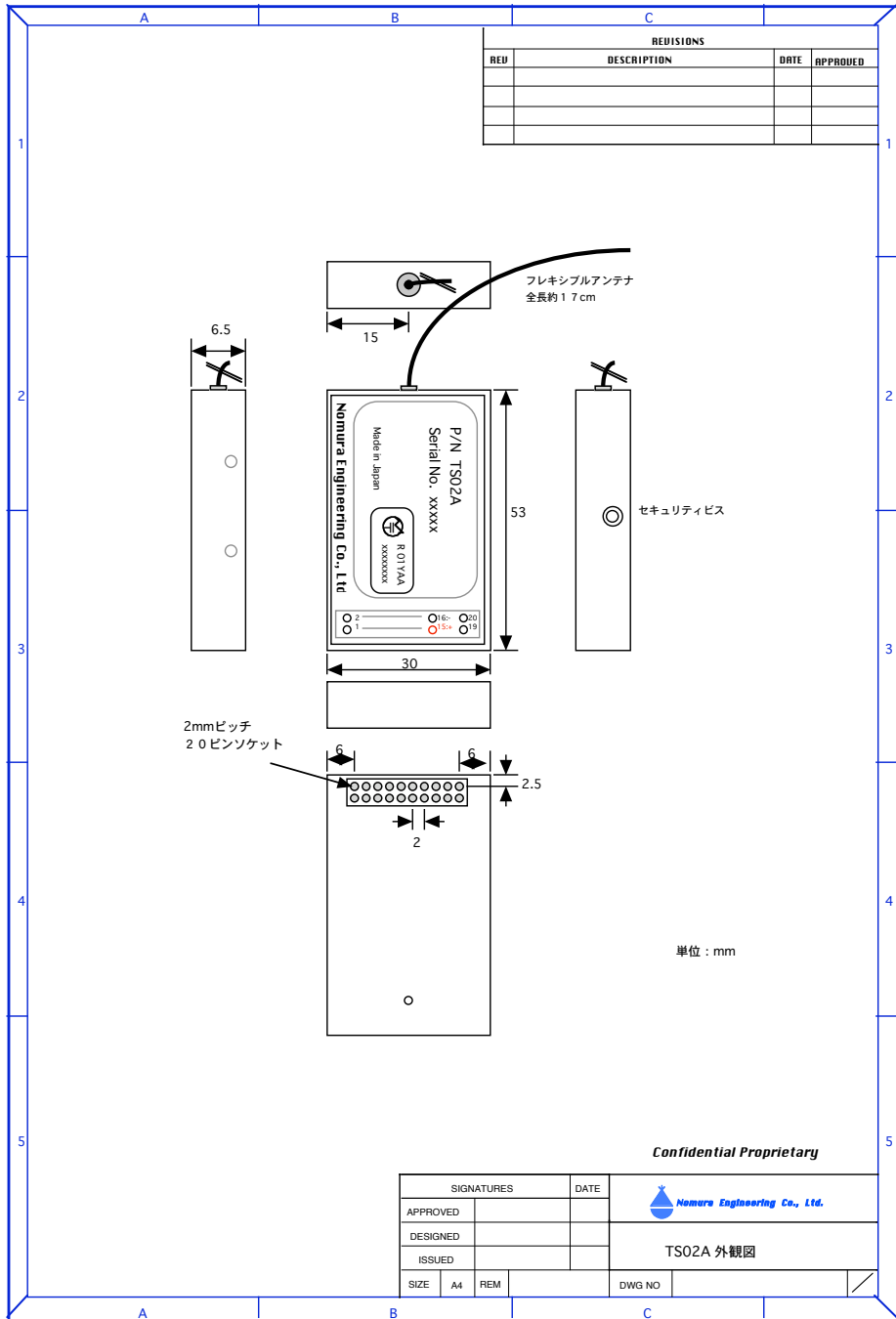
The power supply is supplied with direct current from 2.1 V to 7.0 V. The power noise is eliminated and regulated 2.0 V is output. The output power is TX VCC 2.0 V and RX VCC 2.0 V.

Block Diagram



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Dimensions



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Revision History

Cautions & Warnings

Cautions

Warnings

- Do not disassemble the module.
- Do not remove the label of the module. Use of the product without the label is illegal.